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URGENT

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U.S. PATENT & TRADEMARK OFFICE

Art Unit: 2755
Serial No.: 09/007,019
Filing Date: January 14, 1998
Our Ref No.: 04860.P0686C2

Message:

Examiner Lao:

In response to your telephone call on 9-6-00 to Jim Scheller, attached please find Amendment A as you requested.

Please call us again if you need any further information.

Attorney's Docket No. 04860.P0686C2 *Patent*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Eric C. Anderson
Hugh B. Svendsen

Serial No. 08/478,413

Filed: June 7, 1995

For: Execution Control For Processor Tasks

Examiner: Toplu, L.

Art Unit: 2755

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Applicant respectfully requests the Examiner to enter the following preliminary amendment and consider the following remarks prior to examination of the above referenced patent application.

IN THE CLAIMS

Please amend the following claims:

1. (Amended) A method in a computer system of executing a first sequence of modules in a first task, said first sequence of modules

linked to one another and having at least one sequence of execution, comprising the following steps:

a. storing in each of said first sequence of modules a skip value indicating a next module in said sequence of modules to execute;

b. executing a first module of said first sequence of said modules; and

c. executing said next module of said sequence of modules indicated by the skip value, wherein each module of said sequence of modules comprises at least one digital signal processing data structure.

9. (Twice amended) A method of controlling execution flow of a first task comprising a sequence of first executable modules in a processing system by storing in each of said first executable modules a skip count, said skip count comprising an integer N which indicates that execution should skip to the N+1th module following execution of a currently executed module in the first sequence of executable modules, a value of N less than zero associated with the currently executed module indicating that execution of the first sequence of modules should terminate after completion of execution of the currently executed module, wherein each module comprises at least one digital signal processing data structure.

10. (Amended) A method performed by a processor of controlling the flow of execution of a first set of executable modules sequentially associated with one another comprising the following steps:

a. executing a first module in said first sequence of modules;

b. determining a skip value associated with said first module; and

c. proceeding to execute a subsequent module in said first set of executable modules indicated by said skip value, wherein each module comprises at least one digital signal processing data structure.

16. (Amended) An apparatus for executing a first sequence of modules in a first task, said first sequence of modules linked to one another and having at least one sequence of execution, comprising:

a. means for storing in each of said first sequence of modules a skip value indicating a next module in said sequence of modules to execute;

b. means for executing a first module of said first sequence of said modules; and

c. means for executing said next module of said sequence of modules indicated by the skip value, wherein each module comprises at least one digital signal processing data structure.

17. (Amended) An apparatus for controlling the flow of execution of a first set of executable modules sequentially associated with one another comprising:

a. means for executing a first module in said first sequence of modules;

b. means for determining a skip value associated with said first module; and

c. means for proceeding to execute a subsequent module in said first set of executable modules indicated by said skip value,

wherein each module comprises at least one digital signal processing data structure.

18. (Twice amended) A method of controlling the execution sequence of a series of modules by a processor, each of said modules associated with one another, comprising the following steps:

a. executing the first in said series of modules;

b. determining a skip value N stored in said first in said series of said modules;

c. if the skip value N stored in said first module is less than zero, then terminating the execution of said series of modules;

d. else if the skip value N stored in said first module is greater than or equal to zero then proceeding to a N+1th module in said series of said modules, wherein each of said modules comprises at least one digital signal processing data structure.

19. (Amended) A method in a computer system of performing a first sequence of modules in a first task, said first sequence of modules linked to one another and having at least one sequence of execution, comprising the following steps:

a. storing in a first module of said first sequence of modules a skip value N representing a subsequent module in said first sequence of modules to execute, said skip value N comprising either:

i. an integer less than zero indicating that said first module is a last executable module to be executed in said sequence of modules;

ii. an integer greater than or equal to zero indicating that said process should proceed to said N+1th module subsequent to said first module in said first sequence of said modules;

b. executing the first of said first sequence of said modules; and

c. executing the subsequent module in said sequence of said modules indicated by said skip value, wherein each module of said sequence of modules comprises at least one digital signal processing data structure.

REMARKS

In the Office Action mailed October 14, 1997 on the parent application, claims 1-19 are pending in the application. Claims 1-19 are rejected. Claims 1, 2, 7, 8, 10, 11, and 13-17 are rejected under 35 U.S.C. § 102(e) as being anticipated by Gallagher, U.S. Patent 5, 311, 461 (Gallagher). Claims 3, 9, 12, and 18-19 are rejected under 35 U.S.C. § 103 as being unpatentable over Gallagher in view of Davidson et al., U.S. Patent 4, 893, 234 (Davidson), or Kumar et al., U.S. Patent 5, 197, 137 (Kumar). In response to the above-identified Office Action, Applicants hereby file a Continuation Application pursuant to 37 C.F.R. §1.53(b) accompanied by this Preliminary Amendment, and respectfully request consideration thereof.

Applicants respectfully note that in the Amendment and Response to Office Action filed June 18, 1997 for the parent application, the application was amended to add new claim 20. Thus, claims 1-20 are currently pending in the Continuation Application.

Claims 1, 2, 7, 8, 10, 11, and 13-17 are rejected under 35 U.S.C. § 102(e) as being anticipated by Gallagher. Gallagher discloses using a tree structure priority for resolving conflicting requests for resources. The tree structure consists of pods residing in priority circuitry that can select between two to four resources. Relative priority between resources is represented by a priority code. Each pod comprises a priority circuit (Figure 3, element 19; Figure 4) that is controlled by a programmable set having rotational direction, skip and source identification bits. Each pod is controlled with a priority code that includes a number of bits of data from two up to five bits: two bits for a two-source pod, three for a three-source pod and five bits for a four-source pod where each source is given a code. One of these codes is placed in a pod

as the first two bits of data controlling the pod's priority; the source whose code is placed there will have the highest priority. If this source has a request, it will be processed independent of what the other sources have as a request (column 2, lines 13-29). The priority scheme implemented by the pods disclosed in Gallagher is implemented in priority circuitry that is separate from the resources it controls (column 3, lines 30-33).

Regarding claim 1, the priority scheme implemented by the pods disclosed in Gallagher is implemented in priority circuitry that is separate from the resources it controls. Therefore, each pod of Gallagher comprises only a priority circuit having circuitry for controlling the priority of requests from different processors. As such, Gallagher fails to disclose a sequence of modules linked to one another wherein each module of said sequence of modules comprises at least one digital signal processing data structure. Thus, as Gallagher fails to disclose the claimed invention, amended claim 1 is distinguishable over Gallagher. As amended claims 10, 16, and 17 contain similar limitations to claim 1, amended claims 10, 16, and 17 are distinguishable over Gallagher. As claims 2, 7, 8, 11, and 13-15 depend from amended claims 1 and 10, claims 2, 7, 8, 11, 13-15 are distinguished over Gallagher.

Claims 3, 9, 12, and 18-19 are rejected under 35 U.S.C. § 103 as being unpatentable over Gallagher in view of Davidson or Kumar. Davidson and Kumar both fail to disclose a sequence of modules linked to one another wherein each module of said sequence of modules comprises at least one digital signal processing data structure. As amended claims 9, 18, and 19 contain similar limitations to amended claim 1, amended claims 9, 18, and 19 are distinguished over Gallagher in view of Davidson or Kumar for the same reasons stated above with respect to amended claim 1. As claim 3 depends

from amended claim 1, claim 3 is distinguished over Gallagher. As claim 12 depends from amended claim 10, claim 12 is distinguished over Gallagher.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 1/14, 1998

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